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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,009	12/05/2001	Masao Shinozaki	XA-9590	3040

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MILES & STOCKBRIDGE PC
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MCLEAN, VA 22102-3833

EXAMINER
RAO, SHRINIVAS H

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,009	SHINOZAKI ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *8-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-7 and 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Amendment

Applicants' amendment filed on December 27, 2002 has been entered on January 07, 2003.

Therefore claims 1-7, 21-25 as amended by the amendment are currently pending in the application.

Claim 26 has been cancelled by the amendment.

Election/Restrictions

This application contains claims 8 to 20 drawn to an invention nonelected with out traverse in Paper No. 5 and 8. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Applicants' response in paper 8 (Page 17 lines 1-2) that, " The Examiner is authorized to cancel claims 8 to 20 in order to pass this application to issue "really authorizes the Examiner to cancel claims 8-20 only if the application passes to issue and since the present claims are not patentable i.e the application is not passed to issue, the limited authorization given to the Examiner does not further the prosecution of this application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 to 7 and 21 to 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fifield et al. (U.S. Patent No. 6,166,561 herein after Fifield) in vie w of Etoh et al. (U.S. Patent No. 5,692,999 hereinafter Etoh) previously cited and presently applied.

With respect to claim1, Fifield describes a semiconductor device including an input circuit or an output circuit configured with a plurality of first MOS transistors (fig. 2 # VDD, col. 3 lines 30-32, col. 1 line 39); in a first area of a principal plane on a semiconductor substrate (fig. 2) and an internal circuit configured with a plurality of second MOS transistors in a second area of the principal plane on the semiconductor substrate (fig.2, area # 207 having transistors 219), wherein a first voltage is applied to said plurality of first MOS transistors (Fifield col. 6 lines 60-62) wherein a second voltage smaller than said first voltage is applied to said plurality of second MOS transistors(Fifield col. 6 line 63)

Fifield does not specifically describe a gate length of a first gate electrode of said plurality of first MOS transistors is larger than a gate length of a second gate electrode of said plurality of second MOS transistors.

However Etoh in 14 B and col. 20 lines 50-55, (in fig 14 B gates 51are of larger length than 52) describes a gate length of a first gate electrode of said plurality of first MOS transistors is larger than a gate length of a second gate electrode of said plurality of second MOS transistors to form a low voltage LSI with the performances of high noise resistance, high operation speed and low power consumption.

Therefore it would been obvious to one of ordinary skill in the art at the time of the invention to include Etoh's a gate length of a first gate electrode of said plurality of first MOS transistors is larger than a gate length of a second gate electrode of said plurality of second MOS transistors in Fifield's device to form a low voltage LSI with the performances of high noise resistance, high operation speed and low power consumption. (Etoh col. 20 lines 37-41).

The other limitations of claim 1 are:

and wherein a spacing between said first gate electrode of the first MOS transistors and a first contact hole for connecting a wiring to a source region or a drain region of the first MOS transistors is larger than a spacing between said second gate electrode and a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistors. (Etoh figure 36 c distance between 139 (first electrode) and 142 (contact hole) is larger than the distance between 140 (second electrode) and 144 (second contact hole)).

With respect to claim 2, Fifiled describes a semiconductor device including an input circuit or an output circuit configured with a plurality of first MOS transistors in a first area of a principal plane on a semiconductor substrate, and an internal circuit configured with a plurality of second MOS transistors in a second area of the principal plane on the semiconductor substrate (fig.2, area # 207 having transistors 219), wherein a first voltage is applied to said plurality of first MOS transistors (Fifield col. 6 lines 60-62) wherein a second voltage smaller than said first voltage is applied to said plurality of second MOS transistors(Fifield col. 6 line 63) wherein a spacing between an edge of a

first active region in which the first MOS transistors are formed and a first contact hole for connecting a wiring to a source region or a drain region of the first MOS transistors is larger than a spacing between an edge of a second active region in which the second MOS transistors are formed . (Etoh figure 36 c distance between 139 (first electrode) and 142 (contact hole) is larger than the distance between 140 (second electrode) and 144 (second contact hole)).

With respect to claims 3 and 21, Fifiled describes a semiconductor device including a wherein said input circuit or said output circuit operates with said first voltage and wherein said internal circuit operates with said second voltage (claim 3 , Fifield figs. 4A and B, col. 8 lines 17-48), higher (claim 26, Fifield figs. 4A-B, col. 8 line 49-65).

With respect to claims 4 and 22 Fifiled, describes a semiconductor device wherein said plurality of first MOS transistors are first voltage withstanding MOS transistors and wherein said plurality of second MOS transistors are second voltage withstanding MOS transistors.(Fifield claim 3 , Fifield figs. 4A and B, col. 8 lines 17-48), higher (claim 26, Fifield figs. 4A-B, col. 8 line 49-65).

With respect to claims 5 and 23, a semiconductor device wherein a gate insulating film thickness of the first MOS transistors is larger than a gate insulating film thickness of the second MOS transistors. (Etoh fig. 14 B).

With respect to claims 6 and 24, wherein Fifiled describes a semiconductor device wherein an area of the active region in which the first MOS transistors are

formed is larger than an area of the active region in which the second MOS transistors are formed. (Fifield fig. 3A)

With respect to claims 7 and 25, wherein said plurality of first MOS transistors are p-channel type and the source of each of said plurality of first MOS transistors is supplied with said first voltage a power supply voltage (claim 7 Fifield figs. 4A-B, col. 8 line 49-65), wherein said plurality of second MOS transistors are p-channel (n-channel) type and the source of each of said plurality of second MOS transistors is supplied with said second voltage. (claim 21 Fifield figs. 4A and B, col. 8 lines 17-48) .

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Steven H. Rao

Patent Examiner

February 25, 2003.

LONG PHAM
PRIMARY EXAMINER